Amendments to the Specification:

Please replace paragraph **[0004]** with the following amended paragraph:

[0004] When measured by a current flowing parallel to axis 123, the ~~The~~ resistance of the memory cell 120 differs according to the relative orientations of M1 and M2. When M1 and M2 are anti-parallel (*e.g.*, the logic "0" state), the resistance of the memory cell 120 is at its highest. On the other hand, the resistance of the memory cell 120 is at its lowest when the orientations of M1 and M2 are parallel (*e.g.*, the logic "1" state). Consequently, the logic state of the data bit stored in the memory cell 120 can be determined by measuring, either directly or indirectly, the resistance of the memory cell 120.